

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Application Serial No. .... 09/652,550  
Filing Date ..... August 31, 2000  
Inventor ..... Keiji Jono et al.  
Assignee ..... Micron Technology, Inc. and KMT Semiconductor, LTD  
Group Art Unit ..... 2811  
Examiner ..... T. Tran  
Attorney's Docket No. .... KM1-001  
Title: Methods of Forming an Isolation Trench in a Semiconductor, Methods  
of Forming an Isolation Trench in a Surface of a Silicon Wafer, Methods  
of Forming an Isolation Trench-Isolated Transistor, Trench-Isolated  
Transistor, Trench Isolation Structures Formed in a Semiconductor,  
Memory Cells and DRAMS

**RESPONSE TO OCTOBER 12, 2001 OFFICE ACTION**

To: Box Non-Fee Amendment  
Assistant Commissioner for Patents  
Washington, D.C. 20231

From: Frederick M. Fliegel, Ph.D.  
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Sir:

Responsive to the Office Action dated October 12, 2001<sup>2</sup>, Applicant  
amends and remarks as follows:

**AMENDMENTS**